We Claim:

1. A circuit configuration for controlling load-dependent driver strengths, comprising:

an input terminal for feeding in an input signal;

an output terminal for tapping off an amplified signal;

a first amplifier stage having an input connected to said input terminal for feeding in the input signal and, an output connected to said output terminal for outputting the amplified signal;

a reference circuit receiving the input signal, the amplified signal and a reference voltage, and performing a phase comparison between the input signal and the amplified signal, said reference circuit containing:

a differential amplifier with at least two input terminals receiving the amplified signal and the reference voltage, and outputting a differential output signal;

a logic combination element having a first input receiving the input signal, a second input receiving the

differential output signal of said differential amplifier, and an output; and

a flip-flop having an input connected to said output of said logic combination element and an output outputting a reference output signal; and

a second amplifier stage connected to said output of said flip-flop and having inputs receiving the reference output signal from said reference circuit and the input signal, said second amplifier stage further having an output connected in parallel with said output of said first amplifier stage, and said second amplifier stage switching on in a manner dependent on the reference output signal generated by said reference circuit.

2. The circuit configuration according to claim 1, wherein said differential amplifier compares the reference voltage with a voltage of the amplified signal and has an output outputting the differential output signal.

3. The circuit configuration according to claim 1, wherein said logic combination element compares levels present at said first and second inputs with one another, so that, for a case where a signal with a lower level is present at said second input and a signal with a higher level is present at said

first input, a signal with a high level is generated at said output for driving said flip-flop.

4. The circuit configuration according to claim 1, wherein said flip-flop is set in an event of a signal with a high level being present at said input of said flip-flop and drives said second amplifier stage connected downstream, with a result that said second amplifier stage is switched-on in parallel with said first amplifier stage.

5. The circuit configuration according to claim 1, wherein said second amplifier stage, in an event of being switched-on, effects additional amplification of the input signal.

6. The circuit configuration according to claim 1, wherein the input signal is fed to said logic combination element in a delayed manner.

7. The circuit configuration according to claim 1, wherein said reference circuit further has an additional amplifier stage and a further differential amplifier connected between said additional amplifier stage and said logic combination element, the input signal being fed to said logic combination element through said additional amplifier stage and said further differential amplifier.

8. The circuit configuration according to claim 7, wherein:

said additional amplifier stage outputs an output signal; and

said further differential amplifier has a first input receiving the output signal from said additional amplifier stage and a second input receiving the reference voltage.

9. The circuit configuration according to claim 8, wherein said further differential amplifier has an output and compares the reference voltage with a voltage of the output signal of said additional amplifier stage and outputs a further amplified signal at said output of said further differential amplifier stage.